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APPLICATION

FOR

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TITLE: ELEVATED PORE PHASE-CHANGE MEMORY

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ELEVATED PORE PHASE-CHANGE MEMORY

Background

This invention relates generally to memories that use phase-change materials.

Phase-change materials may exhibit at least two different states. The states may be called the amorphous and crystalline states. Transitions between these states may be selectively initiated in response to temperature changes. The states may be distinguished because the amorphous state generally exhibits higher resistivity than the crystalline state. The amorphous state involves a more disordered atomic structure and the crystalline state involves a more ordered atomic structure. Generally, any phase-change material may be utilized. In some embodiments, however, thin-film chalcogenide alloy materials may be particularly suitable.

The phase-change may be induced reversibly. Therefore, the memory may change from the amorphous to the crystalline state and may revert back to the amorphous state thereafter or vice versa. In effect, each memory cell may be thought of as a programmable resistor that reversibly changes between higher and lower resistance states.

In some situations, a cell may have a large number of states. That is, because each state may be distinguished by its resistance, a number of resistance determined states may be possible, allowing the storage of multiple bits of data in a single cell.

A variety of phase-change alloys are known. Generally, chalcogenide alloys contain one or more elements from column VI of the periodic table. One particularly suitable group of alloys are GeSbTe alloys.

A phase-change material may be formed within a passage or pore defined through a dielectric material. The phase-change material may be coupled to contacts on either end of the passage. State transitions may be induced by applying a current to heat the phase-change material.

An access device may be defined in the substrate of a semiconductor integrated circuit to activate an overlying phase-change material. Other phase-change memory components may also be integrated into the semiconductor substrate. Patterning features over integrated topography may adversely impact the underlying integrated features. Thus, it would be desirable to form the phase-change memory in a fashion, above the rest of the integrated circuit, that does not interfere with any of the previously fabricated integrated structures.

Another issue with phase-change memories is that the greater the heat loss from each memory cell, the greater

the current that must be applied for device programming. Thus, it would be desirable to reduce the amount of heat loss from the heated phase-change material. Similarly, it is desirable to distribute the heat homogenously across the phase-change material. However, many currently proposed techniques result in local variations in device resistance after a programming event. These local variations may also result in stress in local regions during the phase-change programming.

It would be desirable to reduce the cell size as much as possible to thereby reduce product cost. Also it would be desirable to reduce the number of manufacturing steps to the greatest possible extent, to reduce costs.

Thus, there is a need for improved phase-change memories and techniques for making the same.

Brief Description of the Drawings

Figure 1 is an enlarged cross-sectional view of one embodiment of the present invention; and

Figures 2A through 2I are enlarged cross-sectional views of a process for manufacturing the device shown in Figure 1 in accordance with one embodiment of the present invention.

Detailed Description

Referring to Figure 1, a phase-change memory cell 10 may include an elevated pore in accordance with one

embodiment of the present invention. A substrate 12 may include an integrated circuit including access transistors (not shown) that control the current through a base contact 16. A shallow trench isolation structure 14 may isolate the memory cell 10 from the remainder of the structures formed in the substrate 12. Over the substrate 12, is a liner conductor 18 in accordance with one embodiment of the present invention. The liner conductor 18 may be tubular and cup-shaped and may define an open central region that may be filled with a fill insulator 20 in accordance with one embodiment of the present invention. The liner conductor 18 conducts current from the base contact 16 upwardly to an elevated pore.

The elevated pore includes a resistive or lower electrode 22 that may also be tubular and cup-shaped. Within the interior of the lower electrode 22 is a pore defined by a pair of opposed spacers 24 and a phase-change layer 28. The phase-change layer 28 also may be cup-shaped and may be filled with an upper electrode 30 in one embodiment of the present invention. The upper electrode 30 and the phase-change material 28 may be patterned in one embodiment of the present invention.

Referring to Figure 2A, the process of forming the structure shown in Figure 1 begins by forming a pore 34 through an etch stop layer 26 and a dielectric layer 32. The etch stop layer 26 may be of a material that is less

prone to being etched relative to a variety of surrounding layers. In one embodiment, the etch stop layer 26 may be silicon nitride or Si_3N_4.

Moving to Figure 2B, a liner conductor 18 may be deposited within the pore 34 in one embodiment of the present invention. The liner conductor 18 may be titanium, titanium nitride, Tungsten or a combination of these materials in some embodiments. The liner conductor 18 lines the cylindrical pore 34 and may be filled with a fill material 20. Advantageously, the liner conductor 18 is conformal, with consistent coverage on the sidewalls of the pore 34. The fill material 20 provides thermal and electrical isolation. In one embodiment, the fill material 20 may be silicon dioxide.

Turning next to Figure 2C, the structure shown in Figure 2B may be planarized. In one embodiment of the present invention a chemical mechanical planarization (CMP) process may be utilized to create the planar surface indicated as S. The etch stop layer 26 may be used to provide a well controlled final stopping point for the planarization.

As shown in Figure 2D, the fill material 20 is subjected to an etch of controlled distance. Thus, an opening 36 is formed of a controlled depth. In one embodiment of the present invention, the etch of the fill material 20 may be done with a dry insulator etch. This

may be followed by an etch of the liner conductor 18. In one embodiment, the liner conductor 18 may be etched isotropically with minimal overetch. In one embodiment, the liner conductor 18 may be etched using a wet etch following the etch of the fill material 20.

Next, a resistive or lower electrode 22 may be deposited in one embodiment of the present invention, as shown in Figure 2E. The opening 36 in the upper surface of the etch stop 26 may be covered with the lower electrode 22. The electrode 22 may then be covered with an insulator 40. The lower electrode 22 makes an electrical connection to the liner conductor 18 that in turn makes an electrical connection to the contact 16 in the substrate 12.

The structure shown in Figure 2E is then subjected to a planarization process such as CMP, to produce the planarized structure shown in Figure 2F. The liner conductor 18 is then subjected to a recess etch to form the recessed regions indicated at E. In one embodiment, the recess etch may be a short wet etch.

Thereafter, the insulator 40 may be removed using an etching process, such as a dry or wet insulator etch, to produce the pore indicated as F, as shown in Figure 2G, with the lower electrode 22 exposed. Thereafter, a sidewall spacer 24 may be formed as shown in Figure 2H. The spacer 24 may be formed conventionally, for example by depositing an insulator material and then anisotropically

etching the deposited insulator material. In one embodiment, the sidewall spacer 24 may be silicon nitride or silicon dioxide.

Then, as shown in Figure 2I, the structure shown in Figure 2H may be covered by a phase-change layer 28 and an upper electrode layer 30. In one embodiment, the phase-change layer 28 is cup-shaped and extends downwardly into the pore defined by the spacer 24 on the sides and the lower electrode 22 on the bottom. In one embodiment, the phase-change material may be $Ge_2Sb_2Te_5$.

The upper electrode 28 may be a sandwich of a plurality of layers. In one embodiment, the sandwich may include, starting at the bottom, titanium, followed by titanium nitride followed by aluminum.

An electrical connection may be established from the base contact 16 in the substrate 12 through the liner conductor 18 to the lower electrode 22 and then to the phase-change layer 28. Finally in some embodiments, the phase-change layer 28 and upper electrode 30 may be patterned to achieve the structure shown in Figure 1 in some embodiments.

In some embodiments, elevating the pore above the substrate 12 facilitates the integration of the phase-change memory cell into standard complementary metal oxide semiconductor (CMOS) process flows. In particular, elevating the pore avoids patterning features on integrated

circuit topography in the substrate 12. Photolithographic steps may be on planarized surfaces as a result.

In some embodiments, a thermally efficient device structure provides for improved device performance by reducing the required power for device programming. The programmable media volume, represented by the phase-change layer 28, is nearly surrounded by thermal insulation.

The lower electrode 22 provides the heat for producing phase changes at lower currents. The lower electrode 22 may be made relatively thin, reducing heat loss through the electrode 22 in some embodiments. In addition, in some embodiments, temperature distribution is more homogeneous during programming providing for less local variation in device resistance after programming. This structure may also result in developing less stress in local regions when invoking a phase change, in some embodiments.

Likewise, in some embodiments, cell size may be reduced, thereby reducing product cost. Only two additional masking steps may be required to form the structure, in some embodiments, also reducing costs and shortening process cycle times.

While the present invention has been described with respect to a limited number of embodiments, those skilled in the art will appreciate numerous modifications and variations therefrom. It is intended that the appended

claims cover all such modifications and variations as fall within the true spirit and scope of this present invention.

What is claimed is: